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Implementation of H.265/HEVC Standard for Video Applications by Utilizing Multicore Arm Processor

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Abstract

Bandwidth optimization is the key word in the transmission of multimedia data over the internet. The evolution of video compression techniques, video codecs and formats such as AVI, WMV, H.261, H.263, MP4, H.264/AVC etc., has made the data transmission easier. H.265/HEVC is the most recent video standard that has made an enormous leap in the video compression industry. It promises with the delivery of super high quality videos with reduced bitrates and double the compression ratio. This paper proposes the encoding process of a raw YUV video into H.265 standard and to decode it with the readily available H.264 container format.

Keywords: H.265/HEVC, Coding Unit, Prediction Unit, Transform Unit, Macro block, Motion Estimation.

Introduction

In the current scenario with respect to video standards, H.264/AVC is the novel video codec that delivers a High Definition video content for application such as HDTV, Blue Ray etc. In the mid of July 2013, Joint Collaborative Group on Video Coding (JCT-VC) has declared the newest video standard called H.265/HEVC. After a series of performance evaluation the new standard has resulted with 30% bit rate reduction with super high quality video.

The reference software for HEVC codec is HM encoder which is incorporated with all the proficiencies that are required for the final standard. H.265/HEVC is similar to the H.264/AVC standard but, it has many alterations and changes. They have incorporated the Inter and Intra prediction techniques and introduced three new blocking process called Coding Unit including Code tree unit, Prediction Unit and Transform Unit.

Related Work

Numerous video applications exists for different purposes. Each and every application uses different processors, video codecs and standards. Most of the applications are capable of handling the codecs that are readily available right now and those applications has the incapability of handling the H.265/HEVC standard. The objective of this paper is to decode the H.265/HEVC video codec through the multicore ARM processor that promises parallel processing.

A. ARM Processor based Network Media Player

It is a generic embedded streaming media player. It utilizes the single core ARM processor and embedded Linux operating system as platform, and develops an embedded network streaming media player. It can decode the H.264 videos alone and it lacks the hyper threading capability since it uses the single core ARM processors. These kind of media streaming devices are not capable of decoding the latest H.265/HEVC video formats. It is also said that, the compression ratio for H.264 is lesser than the H.265 standard. The bitrate of the decoded video is comparatively larger than the H.265 video standard. The encoding time for the H.264/AVC videos are high and the compression ratio is low, when compared with the HEVC standard. Since the compression ratio for other MPEG formats are not up to the mark, the bitrate for high resolution videos are larger. This leads to enormous consumption of bandwidth. The hardware complexity encoding and decoding process is one of the greatest limitations in other video formats [1].

B. Video Monitoring System

This is an ARM-based low cost video monitoring system. This system has a major drawback of supporting recent codecs such as H.264, H.265. Since, this is a network based video monitoring

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system, the bandwidth consumption would be more because, the bitrate of the existing video formats are higher in order to deliver a high quality videos. As a result, the bandwidth usage is larger [2].

C. 3D Video rendering on multi core architecture

This system focuses on the rendering of 3D video formats that rely on H.264 container format. It decodes and renders on dual-core processors. Format conversion and rendering is also a cycle consuming task which is independent of video decoding. This system is implemented in ARM Cortex-A9 dual core processor. This is a promising technology which utilizes dual core ARM Processor for parallel processing. But the system has a restriction of handling H.265/HEVC video standard and the 3D extension of HEVC. The system can be improvised by adding the HEVC extension for 3D video coding which supports the coding of multiple views and associated depth data [3].

Proposed System

The video coding layer of HEVC is similar to the existing standards since H.261. The input video signal is made into pictures and each pictures are divided into blocks. The first picture of each sequence are coded using intra picture prediction. The consecutive blocks are coded using inter picture prediction and it is done by using Motion Vector for predicting each and every block. The residual signal of the inter and intra picture prediction is the difference of the original and predicted block.

The final picture is stored in the decoder buffer for predicting the consecutive pictures. The order of encoding and decoding process is not synchronized with the arrival of the pictures. The subject video to be encoded undergoes progressive scanning [4]. Some of the unique characteristics and techniques used in H.265/HEVC standard are emphasized in the below sections.

1. Coding Tree Unit(CTU) and Coding Tree Block(CTB)

In the previous standards macro blocks were used for the blocking process and it has a 16 x 16 block containing luma samples and the 4:2:0 color sampling. It has 8 x 8 chroma sample blocks. In the case of HEVC, the macro blocks can be extended upto 64 x 64. The reason for choosing higher rate of blocks is to improvising the compression process [5].

2. Coding Units(CU) and Coding Blocks(CB)

The quad tree format specifies the positions of luma and chroma Coding Blocks. One luma CB and two chroma CB forms the Coding Unit. A Coding Tree Block contains only one Coding Unit and it may have multiple CUs. Each and every CU has Prediction Units and Transform Units [5].

3. Prediction Units(PU) and Prediction Blocks(PB)

The Inter picture prediction and Intra picture prediction is decided at the CU stage. The chroma and luma blocks are further divided on the basis of the previous decisions. The size of the prediction blocks can be varied from 4 x 4 to 64 x 64 samples [5].

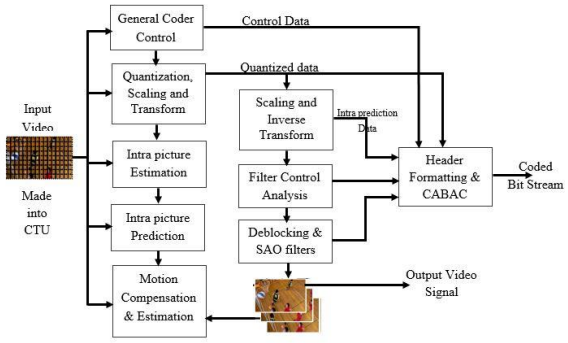

Figure.1 HEVC encoder block

Simulation Scenario

HM reference encoder is used to encode a RAW video file to HEVC video. MS Visual Studio is used to build the HM encoder. With the help of visual studio command prompt, the raw video file is encoded corresponding to the specifications mentioned in the HEVC configuration file. H.264 container format is used to decode the encoded HEVC video file.

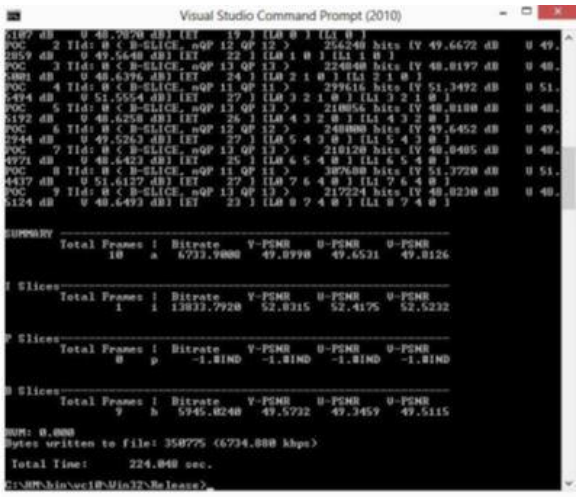

Figure.2 Encoding process using HM encoder

We have obtained a raw output video file that is encoded based on the HEVC configuration. The below figure shows the encoded video

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Figure.3 Encoded video based on HEVC configuration

The encoded video file can be decoded by using H.264 container format. It was done by using a command line converter and the process is shown below.

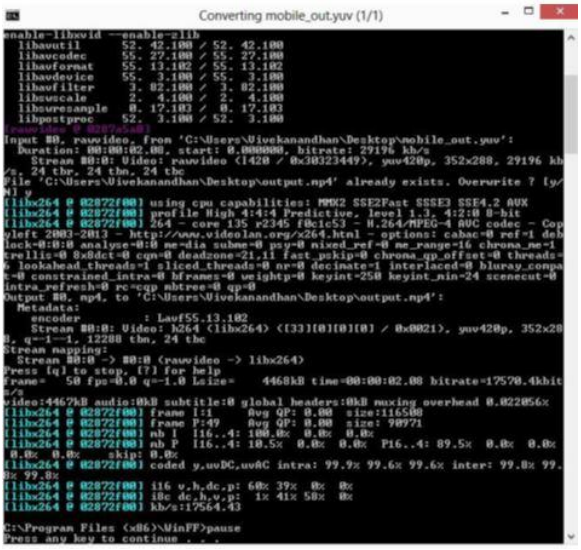

Figure.4 Encoding HEVC raw video in H.264 container format

The encoded video file is decoded by using a client video player called VLC Media Player and it is shown below.

Figure.5 Decoding through client video player.

Conclusion

The raw video footage has been successfully encoded into a H.265/HEVC video with the help of the reference HM encoder and HEVC configurations and decoded with the assistance of H.264 container format. It is a fact that HEVC video can support upto 8K UHD and resolutions up to 8192×4320. It has been already stated that, HEVC standard is versatile towards parallel processing. The forecast of this proposed system is to decode the HEVC video standard through a multicore ARM processor, which greatly suits the applications where hyper threading functionality exists.

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